

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit formed on a single semiconductor chip, comprising:
- a test mode input terminal supplied with a test mode signal;
 - a transmitting circuit having a function of converting first parallel signals for a plurality of channels to a first serial signal;
 - a receiving circuit having a function of converting a second serial signal to second parallel signals for a plurality of channels;
 - a test signal generating circuit responsive to said test mode signal, for generating test parallel signals to be supplied to said transmitting circuit;
 - a first selector for supplying either said test parallel signals generated by said test signal generating circuit or said first parallel signals to said transmitting circuit;
 - a second selector responsive to said test mode signal, for supplying either said first serial signal supplied from said transmitting circuit or said second serial signal to said receiving circuit; and
 - an operation judging circuit responsive to said test mode signal, said operation judging circuit being connected so as to receive response parallel signals from said receiving circuit,
- wherein each of said test parallel signals includes a pulse sequence, and each of said response

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2. A semiconductor integrated circuit according to claim 1, wherein when said test parallel signals constitute such a multi-bit signal that each pulse of a pulse sequence in each of the test parallel signals forms one bit, said first circuit comprises:

a plurality of first flip-flop circuits for sending out said multi-bit test parallel signals;

a plurality of second flip-flop circuits disposed in a stage preceding that of said first flip-flop circuits; and

a plurality of exclusive OR circuits each for comparing values of two bits located at a distance of a predetermined number of bits between and included in bits of the test parallel signals supplied from said plurality of first flip-flop circuits, and supplying a result of the comparison to corresponding one of said plurality of first flip-flop circuits.

3. A semiconductor integrated circuit according to claim 2, wherein said operation judging circuit comprises an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits.

4. A semiconductor integrated circuit according to claim 2, wherein said operation judging circuit comprises:

an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits;

a third flip-flop circuit for taking in an output of said AND circuit in synchronism with a clock signal; and

an SR latch circuit that is set by an output of said third flip-flop circuit.

5. A semiconductor integrated circuit according to claim 2, wherein said operation judging circuit

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comprises:

an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits;

a third flip-flop circuit for taking in an output of said AND circuit in synchronism with a clock signal;

an SR latch circuit that is set by an output of said third flip-flop circuit; and

a reset circuit for canceling a reset state of said SR latch circuit upon elapse of a predetermined time after a circuit disposed in a stage preceding that of said SR latch circuit is reset.

6. A semiconductor integrated circuit according to claim 1, wherein said test signal generating circuit and said operation judging circuit are formed so as to operate in accordance with a clock having a frequency corresponding to a transfer rate of said first or second parallel signals.

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